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EXAMINER

KENNEDY, ADRIAN L

ART UNIT PAPER NUMBER

2121

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/710,885	Applicant(s) LORENZ ET AL.	
	Examiner Adrian L. Kennedy	Art Unit 2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-41 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-41 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/30/05</u> . | 6) <input type="checkbox"/> Other: _____ |

Examiner's Detailed Office Action

1. This Office Action is responsive to application 10/710,885, filed **August 10, 2004**.
2. **Claims 1-41** have been examined.

Information Disclosure Statement

3. Applicants are respectfully reminded of the ongoing Duty to disclose 37 C.F.R. 1.56 all pertinent information and material pertaining to the patentability of applicant's claimed invention, by continuing to submit in a timely manner PTO-1449, Information Disclosure Statement (IDS) with the filing of applicant's application or thereafter.

Specification

4. The abstract of the disclosure is objected to because abstracts are required to be no longer the 15 lines of text and must contain 50-150 words only. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. The invention as disclosed in claims 1-41 are directed to non-statutory subject matter i.e., an abstract idea. Regarding claims 1-41, the applicant is reminded that "*the claimed invention as a whole must accomplish a practical application. That is it must produce a 'useful, concrete and*

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tangible result’.” *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02, MPEP § 2106 [R-3]

(II-A)

Applicants’ claimed invention of claims 1-41 sets forth a system but fails to disclose any tangible real world result that is produced by that system. Reading applicants’ claims in light of the specification, no limit is placed upon the method of representing the system, since applicants have presented a series of non-limiting examples of what the invention could be without specifying exactly what the invention is. The examiner takes the position that the applicants’ claimed invention could be driven to an actual computer, but could also be driven to a digital circuit or a model of the system disclosed.

Claims 20-41 are considered to be an algorithm which does not produce a tangible real world result. Accordingly, these claims are not considered to embody patent eligible matter.

7. Quoting *Diamond V. Diehr* and *Lutton*, 209 USPQ 1 (US SupCt 1981):

*...the definition of “process” announced by this Court in *Cochrane v. Deener* 94 U.S. 780, 787-788 (1876), seemed to indicate that a patentable process must cause a physical transformation in the materials to which the process is applied. See ante, at 7-8, 209 USPQ at 6*

8. Therefore, claims 1-41 are rejected under 35 USC § 101.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-41 are considered to be indefinite. Reading applicants’ disclosure, the claims having been read in light thereof, it is not clear what applicants’ invention is directed to. While

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applicants have provided potential examples, applicants have not particularly pointed out and distinctly claimed that which is their invention. A statement of what the invention could be or examples of what the invention might be does not provide an adequate description of what the applicants have invented.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1-3, 20-22, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of Gerstenmaier *et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984.

Regarding claim 1:

Zahn teaches

A system for evaluation of a set of rules based on input data, the system comprising:

a rules interface for receiving a set of rules [C 4, L 6-9; “*rule processing*”], each rule having at least one condition [C 5, L 4-6; “*rule conditions*”];

a network builder [C 5, L 32-35; “*Rule editor*”] for building a Boolean Network representation of the set of rules, the Boolean Network representation including generating a Boolean value based on evaluating an item of input data against a condition of a rule [C 5, L 4-7]; and

a runtime evaluation engine for receiving input data [C 5, L 7-9; “*Inference Engine*”], detecting changed items of input data [C 6, L 60-63], activating links [C 6, L 22-24; The examiner takes the position that the operations of “run” and “halt” of the Altered Event Class are fully capable of activating or deactivating links] based on said changed items of input data [C 6, L 60-63] so as to utilize the Boolean Network representation relevant to rule evaluation outcome, and evaluating rules based on the input data and active transducers and logic gates of the Boolean Network representation [C 2, L 35-37].

Zahn fails to teach transducers linked by logic gates. However, Gerstenmaier et al. does teach transducers linked by logic gates [*Gerstenmaier et al.* (USPN 4,475,159); C 3, L 31-34].

In the book *Structured Computer Organization*, Tanenbaum states, “*Hardware and software are logically equivalent.*” As a result of this teaching, the examiner takes the position that it would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of Zahn (USPN 6,535,864) with the invention of

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Gerstenmaier et al. (USPN 4,475,159), for the purpose of assuring the delivery of a signal [*Gerstenmaier et al.* (USPN 4,475,159); C 4, L 20-24].

Regarding claim 2:

Zahn fails to teach the system wherein logic gate include OR gates.

However, *Gerstenmaier et al.* teaches

The system wherein said logic gates of the Boolean Network representation include OR gates [C 4, L 20-24].

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of *Zahn* (USPN 6,535,864) with the invention of *Gerstenmaier et al.* (USPN 4,475,159), for the purpose of assuring the delivery of a signal [*Gerstenmaier et al.* (USPN 4,475,159); C 4, L 20-24].

Regarding claim 3:

Zahn fails to teach the system wherein logic gates include conjunctive logic gates and disjunctive logic gates.

However, *Gerstenmaier et al.* teaches

The system wherein said logic gates of the Boolean Network representation include conjunctive logic gates [C 3, L 31-34; "AND"] and disjunctive logic gates [C 3, L 31-34; "OR"].

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of *Zahn* (USPN 6,535,864) with the invention of *Gerstenmaier et*

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al. (USPN 4,475,159), for the purpose of assuring the delivery of a signal [*Gerstenmaier et al.* (USPN 4,475,159); C 4, L 20-24].

Regarding claim 20:

Zahn teaches

A method for evaluating a set of rules based on input data, the method comprising:

- receiving a set of rules [C 4, L 6-9; “*rule processing*”], each rule having at least one condition [C 5, L 4-6; “*rule conditions*”];
- building a Boolean Network representation of the set of rules [C 5, L 32-35; “*Rule editor*”], the Boolean Network representation including generating a Boolean value based on evaluating an item of input data against a condition of a rule [C 5, L 4-7];
- detecting changed items of input data [C 6, L 60-63; “*change of state*”];
- in response to changed items of input data, activating links [C 3, L 49-50; “*reference is a link*”] of the Boolean Network representation so as to utilize the Boolean Network representation relevant to rule evaluation outcome; and
- determining results of the set of rules based on the input data of the Boolean Network representation [C 2, L 35-37].

Zahn fails to teach transducers linked by logic gates. However, Gerstenmaier et al. does teach transducers linked by logic gates [*Gerstenmaier et al.* (USPN 4,475,159); C 3, L 31-34]

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In the book *Structured Computer Organization*, Tanenbaum states, “*Hardware and software are logically equivalent.*” As a result of this teaching, the examiner takes the position that it would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) with the invention of *Gerstenmaier et al.* (USPN 4,475,159), for the purpose of assuring the delivery of a signal [*Gerstenmaier et al.* (USPN 4,475,159); C 4, L 20-24].

Regarding claim 21:

Zahn fails to teach the system wherein logic gate include OR gates.

However, Gerstenmaier et al. teaches

The method wherein said logic gates of the Boolean Network representation include OR gates [C 4, L 20-24].

Regarding claim 22:

Zahn fails to teach the system wherein logic gates include conjunctive logic gates and disjunctive logic gates.

However, Gerstenmaier et al. teaches

The method wherein said logic gates of the Boolean Network representation include conjunctive logic gates [C 3, L 31-34; “AND”] and disjunctive logic gates [C 3, L 31-34; “OR”].

Regarding claim 40:

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Zahn teaches

A computer-readable medium having processor-executable instructions [C 8, L 35-41].

Regarding claim 41:

Zahn teaches

A downloadable set of processor-executable instructions [C 8, L 35-41].

14. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984 and further in view of *Chan* (USPN 7,065,745), Filed: December 16, 2002; Date of Patent: June, 20, 2006.

Regarding claim 4:

Zahn in combination with Gerstenmaier et al. does not teach the system wherein the rules interface receives rule written in RuleML.

However, Chan teaches

The system wherein said rules interface receives rules written in RuleML [C 6, L 55-60; “RuleML”].

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Chan* (USPN 7,065,745) for the purpose of “implementing rules” [*Chan* (USPN 7,065,745); C 6, L 55-60].

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Regarding claim 23:

Zahn in combination with Gerstenmaier et al. does not teach the method wherein said receiving step includes receiving a set of rules written in RuleML.

However, Chan teaches

The method wherein said receiving step includes receiving a set of rules written in RuleML [C 6, L 55-60; "*RuleML*"].

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Chan* (USPN 7,065,745) for the purpose of "*implementing rules*" [*Chan* (USPN 7,065,745); C 6, L 55-60]

15. Claims 5 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984 and further in view of *Java* (<http://jcp.org/en/jsr/detail?id=94>), Date of Specification: December 5, 2000.

Regarding claim 5:

Zahn in combination with Gerstenmaier et al. does not teach the system wherein said rules interface comprises a JSR 94 interface.

However, Java teaches

The system wherein said rules interface comprises a JSR 94 interface [*Java*].

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The examiner takes the position that the use of JSR 94 or the Java Rule Engine API would have been obvious to one skilled in the art at the time of invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Java* for the purpose of facilitating the input of rules (*Java*; “*input to a rule engine is a collection of rules*”). As obtained from the Java website, the original specification (JSR 94) for the Java Rule Engine was made public on December 5, 2000 as cited on the Java Specification Request Website.

Regarding claim 24:

Zahn in combination with *Gerstenmaier et al.* does not teach the method wherein said receiving step includes a set of rules through a JSR 94 interface.

However, *Java* teaches

The method wherein said receiving step includes receiving a set of rules through a JSR 94 interface [*Java*].

The examiner takes the position that the use of JSR 94 or the Java Rule Engine API would have been obvious to one skilled in the art at the time of invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Java* for the purpose of facilitating the input of rules (*Java*; “*input to a rule engine is a collection of rules*”). As obtained from the Java website, the original specification (JSR 94) for the Java Rule Engine was made public on December 5, 2000 as cited on the Java Specification Request Website.

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16. Claims 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984 and further in view of *Rostoker et al.* (USPN 6,470,482), Filed: August 5, 1996; Date of Patent: October 22, 2002.

Regarding claim 6:

Zahn in combination with *Gerstenmaier et al.* does not teach the system wherein the network builder factors the set of rules for common expression so as to remove redundancies.

However, *Rostoker et al.* teaches

The system wherein said network builder factors the set of rules for common expressions so as to remove redundancies [C 16, L 9-11; “*removing redundancies*”] from the Boolean Network representation.

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Rostoker et al.* (USPN 6,470,482) for the purpose of “*logic optimization*” [C 16, L 6-7].

Regarding claim 25:

Zahn in combination with *Gerstenmaier et al.* does not teach the method wherein the building step includes factoring the set of rules for common expression so as to remove redundancies

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However, Rostoker et al. teaches

The method of claim 20, wherein said building step includes factoring the set of rules for common expressions so as to remove redundancies [C 16, L 9-11; “*removing redundancies*”] from the Boolean Network representation.

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Rostoker et al.* (USPN 6,470,482) for the purpose of “*logic optimization*” [C 16, L 6-7].

17. Claims 7, 8, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984 and further in view of *Keats* (USPN 4,048,483), Filed: July 23, 1976; Date of Patent: September 13, 1977.

Regarding claim 7:

Zahn in combination with *Gerstenmaier et al.* does not teach the system wherein the network builder creates groups of related transducers so as to provide for more efficient evaluation of data.

However, *Keats* teaches

The system wherein said network builder creates groups of related transducers [C 2, L

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12-14; “*groups of n transducers*”] so as to provide for more efficient evaluation of input data.

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Keats* (USPN 4,048,483) for the purpose of providing “*redundancy*” [C 1, L 11-15]. The examiner takes the position that providing redundancy increases efficiency in the invention of Keats by decreasing the data handling system’s downtime.

Regarding claim 8:

Zahn in combination with *Gerstenmaier et al.* does not the system wherein related transducers comprise transducers evaluating a common item of input data.

However, *Keats* teaches

The system wherein said related transducers [C 2, L 12-14; “*groups of n transducers*”] comprise transducers evaluating a common item of input data [C 1, L 11-15, “*replicate both the input data channels*”].

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Keats* (USPN 4,048,483) for the purpose of providing “*redundancy*” [C 1, L 11-15]. The examiner takes the position that providing redundancy increases efficiency in the invention of Keats by decreasing the data handling

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system's downtime.

Regarding claim 26:

Zahn in combination with Gerstenmaier et al. does not teach the method wherein said building step includes grouping related transducers so as to provide for more efficient evaluation for input data.

However, Keats teaches

The method wherein said building step includes grouping related transducers [C 2, L 12-14; "*groups of n transducers*"] so as to provide for more efficient evaluation of input data.

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of Zahn (USPN 6,535,864) and Gerstenmaier et al. (USPN 4,475,159) with the invention of Keats (USPN 4,048,483) for the purpose of providing "*redundancy*" [C 1, L 11-15]. The examiner takes the position that providing redundancy increases efficiency in the invention of Keats by decreasing the data handling system's downtime.

Regarding claim 27:

Zahn in combination with Gerstenmaier et al. does not teach the method wherein said step of grouping related transducers includes grouping transducers evaluating common items of input data.

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However, Keats teaches

The method wherein said step of grouping related transducers [C 2, L 12-14; “*groups of n transducers*”] includes grouping transducers evaluating a common item of input data [C 1, L 11-15, “*replicate both the input data channels*”].

It would have been obvious to one skilled in the art at the time of applicants’ invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Keats* (USPN 4,048,483) for the purpose of providing “*redundancy*” [C 1, L 11-15]. The examiner takes the position that providing redundancy increases efficiency in the invention of Keats by decreasing the data handling system’s downtime.

18. Claims 9 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984, in view of *Keats* (USPN 4,048,483), Filed: July 23, 1976; Date of Patent: September 13, 1977 and further in view of *Montfort et al.* (USPN 6,205,315), Filed: November 24, 1999; Date of Patent: March 20, 2001.

Regarding claim 9:

Zahn in combination with *Gerstenmaier et al.* and *Keats* does not teach the system wherein the groups of related transducers are grouped based on transducer condition.

However, *Montfort et al.* teaches

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The system wherein said groups of related transducers are grouped based on transducer condition [C 9, L 34-38; "*group of identical transducers*"].

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of *Zahn* (USPN 6,535,864), *Gerstenmaier et al.* (USPN 4,475,159) and *Keats* (USPN 4,048,483) with the invention of *Montfort et al.* (USPN 6,205,315) for the purpose of providing a uniform response amongst the transducers [C 2, L 58-59]

Regarding claim 28:

Zahn in combination with *Gerstenmaier et al.* and *Keats* does not teach the system wherein the groups of related transducers based on conditional operator of said transducers.

However, *Montfort et al.* teaches

The method wherein said grouping of related transducers further comprises grouping related transducers based on conditional operator of said related transducers [C 9, L 34-38; "*group of identical transducers*"].

It would have been obvious to one skilled in the art at the time of applicants' invention to combine the invention of *Zahn* (USPN 6,535,864), *Gerstenmaier et al.* (USPN 4,475,159) and *Keats* (USPN 4,048,483) with the invention of *Montfort et al.* (USPN 6,205,315) for the purpose of providing a uniform response amongst the transducers [C 2, L 58-59]

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19. Claims 11 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Zahn* (USPN 6,535,864), Filed: August 5, 1999; Date of Patent: March 18, 2003 in view of *Gerstenmaier et al.* (USPN 4,475,159), Filed: January, 9, 1982; Date of Patent: October 2, 1984 and further in view of *Harik et al.* (USPubN 2004/0068697), Filed: September 30, 2003; Published: April 8, 2004

Regarding claim 11:

Zahn in combination with *Gerstenmaier et al.* does not teach the system wherein the network builder assigns weights to links between nodes of the Boolean Network representation for establishing an order in which transducers and logic gates are activated.

However, *Harik et al.* teaches

The system wherein said network builder assigns weights to links [Page 14, Section 0222; “*link weight*”] between nodes of the Boolean Network [P 7, S 0115; “*Boolean node network*”] representation for establishing an order in which transducers and logic gates are activated.

It would have been obvious to one of ordinary skill in the art at the time of applicant’s invention to combine the invention of *Zahn* (USPN 6,535,864) and *Gerstenmaier et al.* (USPN 4,475,159) with the invention of *Harik et al.* (USPubN 2004/0068697) for the purpose of creating a Boolean network [P 7, S 0115; “*Boolean node network*”].

Regarding claim 30:

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Zahn in combination with Gerstenmaier et al. does not teach the method wherein said building step includes assigning weights to links between nodes of the Boolean Network representation for establishing an order in which transducers and logic gates are activated.

However, Harik et al. teaches

The method wherein said building step includes assigning weights to links [P 14, S 0222; “*link weight*”] between nodes of the Boolean Network [P 7, S 0115; “*Boolean node network*”] representation for establishing an order in which transducers and logic gates are activated.

It would have been obvious to one of ordinary skill in the art at the time of applicant’s invention to combine the invention of Zahn (USPN 6,535,864) and Gerstenmaier et al. (USPN 4,475,159) with the invention of Harik et al. (USPubN 2004/0068697) for the purpose of creating a Boolean network [P 7, S 0115; “*Boolean node network*”].

20. Claims 10, 12-19, 29 and 31-39 which are not rejected under the prior arts, would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st paragraph and U.S.C 101, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter: Claim 10 is allowable subject matter because the prior art of the record fails to teach or fairly suggest in combination with the other elements and features the grouping of transducers based on the transducers’ condition, the examiner was not able to find any

reference that taught implying or inferring a evaluation result based on related transducers.

Claims 12 and 29 are allowable because the prior art of the record fails to teach or fairly suggest in combination with the other elements and features the use of active transducers and the activation of transducers and logic gates based on the evaluation of data input and link weights.

Claims 13-19, 31-33 and 39 are allowable because the prior art of the record fails to teach or fairly suggest in combination with the other elements and features the specific information of these claims. This is due to the limiting nature of the scope of the claims, especially when referring to specific links and specific types of logic gates.

Claims 34, 36 and 38 are allowable because the prior art of the record fails to teach or fairly suggest in combination with the other elements and features the propagation of activation messages from AND gates back through logic nodes and transducers.

Claims 35 and 37 are allowable because the prior art of the record fails to teach or fairly suggest in combination with the other elements and features the passivating of links.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. *Hill et al.* (USPN 3,846, 745) is cited for his electronic scanning switch that makes use of groups of transducers. *Peller* (USPN 6,882,181) is cited for his data bus with a plurality of nodes. *Keeler et al.* (USPN 6,363,289) is cited for his residual activation neural network. *Haley* (USPubN 2004/0030421) is cited for a system for knowledge management and

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automation. *Chan* (USPubN 2004/0117765) is cited for a system and method for evaluating and executing a hierarchy of rules. *Szabo* (USPN 5,966,126 and USPN 6,326,962) is cited for a graphic user interface database system. *Whitaker et al.* (USPN 6,993,731) is cited for his optimization of digital designs. *Whitaker et al.* (2003/0126579) is cited for his digital design using a selection operation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adrian L. Kennedy whose telephone number is (571) 272-5933. The examiner can normally be reached on Mon -Fri 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on (571) 272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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